What Is Claimed Is:

1. A video compression system, comprising:

a processor-based platform coupled to a bus subsytem; and

coupled to the bus subsystem, a front end subsystem having at least a DCT/IDCT module coupled to a motion estimation and compensation engine (MEC engine) and to a quantizer/inverse-quantizer (Q/Q^{-1}) module.

2. The video compression system according to Claim 1, wherein the DCT/IDCT module includes:

a plurality of cores, each of said cores accepting input data and each of said cores generating output data; and

a sequence generator receiving control signals from the bus subsystem and in response thereto generating a plurality of control signals for each of said cores.

3. The video compression system according to Claim 2, wherein the plurality of cores comprises eight cores.

4. The video compression system according to Claim 2, wherein the plurality of cores comprises four types of cores.

5. The video compression system according to Claim 4, wherein a first type of core includes a main register for storing the input data and feedback data.

6. The video compression system according to Claim 4, wherein a second type of core includes a first pair of lookup tables, and a third type of core includes a second pair of lookup tables.

7. The video compression system according to Claim 6, wherein the second and third types of cores each includes a temporary buffer, and the first and second pairs of lookup tables each includes a 16-bit lookup table and a 12-bit lookup table.

8. The video compression system according to Claim 7, wherein the first pair of lookup tables are selected to provide partial pixel values according to

$$V_i = A_3c + A_2 2^{-4} c + b,$$

wherein V_i represents an intermediate DCT value, A_3 and A_2 are 4-bit binary numbers, c is a constant cosine coefficient, and b is a common coefficient.

9. The video compression system according to Claim 8, wherein the V_i is stored in the temporary buffer for further DCT processing.

10. The video compression system according to Claim 4, wherein a fourth type of core includes two pairs of lookup tables.

11. The video compression system according to Claim 10, wherein the two pairs of lookup tables includes two 16-bit lookup tables and two 12-bit lookup tables.

12. The video compression system according to Claim 10, wherein the two pairs of lookup tables are selected to provide partial pixel values according to

$$\text{result} = A_1 2^{-8} c + A_0 2^{-12} c + V_i,$$

wherein A_1 and A_0 are 4-bit binary numbers.

13. The video compression system according to Claim 4, wherein the input data for each core includes external data and output data from four other cores.

14. The video compression system according to Claim 13, wherein the external data comprises a datablock of prediction data processed by the MEC engine.

15. The video compression system according to Claim 2, wherein said output data from each core is selectively provided as a portion of the input data to other cores.

16. The video compression system according to Claim 15, wherein a portion of the input data is received from one of the MEC engine and the Q/Q^{-1} module.

17. A DCT/IDCT circuit for enabling forward and inverse discrete cosine transform of a datablock, comprising:

a plurality of cores, each having input data and output data, wherein the input data for each core includes external data and output data feedback from selected ones of the cores.

18. The DCT/IDCT circuit according to Claim 17, further comprising:

a sequence generator coupled to each core.

19. The DCT/IDCT circuit according to Claim 17, wherein the selected ones of the cores comprises four cores.

20. The DCT/IDCT circuit according to Claim 17, wherein the external data comprises the datablock, the datablock including prediction data processed by an MEC engine communicatively coupled to the DCT/IDCT circuit.

21. The DCT/IDCT circuit according to Claim 17, wherein the external data comprises the datablock, the datablock including reconstruction data processed by an inverse quantizer module communicatively coupled to the DCT/IDCT circuit.

22. The DCT/IDCT circuit according to Claim 17, wherein the plurality of cores comprises 8 cores.

23. The DCT/IDCT circuit according to Claim 17, wherein the

plurality of cores comprises four types of cores.

24. The DCT/IDCT circuit according to Claim 23, wherein a first type of core includes a main register for storing the input data and feedback data.

25. The DCT/IDCT circuit according to Claim 23, wherein a second type of core includes a first pair of lookup tables, and a third type of core includes a second pair of lookup tables.

26. The DCT/IDCT circuit according to Claim 23, wherein a fourth type of core includes two pairs of lookup tables.

27. A DCT circuit enabling forward discrete cosine transform of a datablock, comprising:

a plurality of cores, each having input data and output data, wherein the input data for each core includes external data and output data feedback from selected ones of the cores.

28. The DCT circuit according to Claim 27, further comprising:

a sequence generator coupled to each core.

29. The DCT circuit according to Claim 27, wherein the selected ones of the cores comprises four cores.

30. An IDCT circuit enabling inverse discrete cosine transform of a datablock, comprising:

a plurality of cores, each having input data and output data, wherein the input data for each core includes external data and output data feedback from selected ones of the cores.

31. The IDCT circuit according to Claim 30, further comprising:

a sequence generator coupled to each core.

32. The IDCT circuit according to Claim 30, wherein the selected ones of the cores comprises four cores.

33. A video processing system, comprising:

a processor-based platform coupled to a bus subsytem; and

coupled to the bus subsystem, a front end subsystem having at least a circuit including

a plurality of cores, each of said cores accepting input data and each of said cores generating output data; and

a sequence generator receiving control signals from the bus subsystem and in response thereto generating a plurality of control signals for each of said cores.

34. The video processing system according to Claim 33, further comprising:

a motion estimation and compensation engine and a quantizer/inverse-quantizer (Q/Q-1) module both communicatively coupled to the circuit.

35. The video processing system according to Claim 33, wherein the input data for each core includes external data and output data feedback from selected ones of the cores remaining.

36. The video processing system according to Claim 35, wherein the plurality of cores comprises eight cores.

37. The video processing system according to Claim 33, wherein the circuit comprises one of a DCT circuit, an IDCT circuit, and a DCT/IDCT circuit

38. A DCT/IDCT circuit for enabling forward and inverse discrete cosine transform of a datablock, comprising:

means for selecting one of input data of the datablock received and a sum of said input data and feedback data in order to provide first output data;

coupled to the means for selecting, means for determining first partial products based on the input data, the first output data and the feedback data;

coupled to the means for selecting and the means for determining first

partial products, means for determining an intermediate result based on a sum of the first partial products; and

coupled to the means for selecting, the means for determining first partial products, and the means for determining an intermediate result, means for providing the intermediate result as an operand added to second partial products to obtain a final result.

39. The DCT/IDCT circuit according to Claim 38, further including means for obtaining the final result within two clock cycles.

40. A DCT/IDCT circuit for enabling forward and inverse discrete cosine transform of a datablock, comprising:

means for receiving input data associated with the datablock;

coupled to the means for receiving, first means for selecting one of the input data and a sum of the input data and feedback data to provide first output data;

coupled to the first means, second means for determining a sum of first partial products based on the input data, the feedback data, and first coefficient data to provide second output data;

coupled to the means for receiving input data, third means for determining a sum of second partial products based on the input data, the feedback data, and second coefficient data to provide third output data;

coupled to the means for receiving input data, fourth means for determining a sum of additional partial products based on the input data, the feedback data, and additional coefficient data to provide third output data; and

means for outputting the first output data, the second output data and the third output data collectively representing a result of one of the forward discrete cosine transform and the inverse discrete cosine transform.